64. (Newly Added) The test device according to claim 63, wherein

the integrated circuits include voltage generating circuits, respectively, for application of the potentials to the potential application terminals provided in the integrated circuits, and

the control signal for shutting off application of the potential to the potential application terminal of the integrated circuit from which the output data having the defect is output is supplied from a voltage generating circuit of the integrated circuit from which the output data having the defect is output to the control circuit of the integrated circuit from which the output data having the defect is output.

65. (Newly Added) The test device according to claim 62, wherein

the output data output from the dedicated output terminals of the at least two of the integrated circuits are potentials therein, and

the judgment circuit determines whether a variation in potential in each of the at least two of the integrated circuits detected by the detection circuit falls within a predetermined range of allowance.

66. (Newly Added) The test device according to claim 62, wherein the test device tests two or more of the semiconductor integrated circuit devices simultaneously and in parallel.

67. (Newly Added) The test device according to claim 65, wherein the test device tests two or more of the semiconductor integrated circuit devices simultaneously and in parallel

REMARKS

The Office Action mailed June 6, 2002 has been carefully reviewed and the foregoing amendments and the following remarks are made in response thereto.

The title stands objected to as not being clearly indicative of the invention to which the claims are directed. Claims 34 and 36-40 stand rejected under 35 U.S.C. § 112, second paragraph as being indefinite for failing to particularly point out and distinctly

claim the subject matter which Applicant regards as the invention. Claims20, 22-27 and 29-33 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,473,183 to Yonemoto. Claims 21, 28 and 35 have been allowed.

By this amendment, a new title has been submitted that is clearly indicative of the invention to which the claims are directed. Claims 20, 22-27, 29-34 and 36-40 have been canceled without prejudice to or disclaimer of the subject matter contained therein. Thus, the above rejections of these claims have been rendered moot. New claims 41-67 have been added. Allowed claims 21, 28 and 35 remain unchanged. Thus, claims 21, 28, 35 and 41-67 are presently pending in this application for consideration.

Applicant respectfully submits that new claims 41-67 are patentably distinguishable over the Yonemoto reference as required by §102. Applicant further submits that the Yonemoto reference fails to disclose or suggest: (1) "at least two first well regions of a second conductivity type formed in a semiconductor substrate of a first conductivity type, and at least one second well region of the first conductivity type formed in at least two first well regions...with semiconductor elements formed in the at least two first well regions and the at least one second well region and a memory circuit comprising the semiconductor elements" as recited in independent claim 41 and (2) "at least two first well regions of a second conductivity type formed in a semiconductor substrate of a first conductivity type, and integrated circuits formed on the at least two first well regions, respectively, which have different functions" as recited in independent claims 42, 56 and 62. Thus, claims 41, 42, 56 and 62 and all claims dependent directly or indirectly therefrom are allowable. These distinctions will be described in greater detail below.

THE CLAIMS DISTINGUISH OVER THE CITED REFERENCE

The present application relates to a semiconductor integrated circuit device including a plurality of circuits having different functions. According to one embodiment of the present invention, the semiconductor integrated circuit includes a semiconductor substrate of a first conductivity type. At least two first well regions of a second conductivity type are formed in the semiconductor substrate and at least one second well region of the first conductivity type is formed in the at least two first well regions. The semiconductor integrated circuit device has semiconductor elements formed in the at least

two first well regions and the at least one second well region and a memory circuit includes the semiconductor elements.

According to another embodiment of the present invention, the semiconductor integrated circuit device includes a semiconductor substrate of a first conductivity type. At least two first well regions of a second conductivity type are formed in the semiconductor substrate. Integrated circuits are formed on the at least two first well regions, respectively, and have different functions.

New independent claims41 specifically recites the arrangement of "at least two first well regions of a second conductivity type formed in a semiconductor substrate of a first conductivity type, and at least one second well region of the first conductivity type formed in at least two first well regions...with semiconductor elements formed in the at least two first well regions and the at least one second well region and a memory circuiting comprising the semiconductor elements" and new independent claims 42, 56 and 62 specifically recite the arrangement of "at least two first well regions of a second conductivity type formed in a semiconductor substrate of a first conductivity type, and integrated circuits formed on the at least two first well regions, respectively, which have different functions". Applicant respectfully submits that the Yonemoto reference fails to disclose or suggest these claimed arrangements.

The Yonemoto reference is directed to a semiconductor device for use with a complementary metal oxide semiconductor (CMOS) inverter in a peripheral circuit of an image sensor. FIGS. 3 and 4 of Yonemoto illustrate CMOS converters. In FIG. 3, the CMOS converter includes one P-type well formed in an N-type substrate, one N-type well formed in the P-type well, one P-type FET formed in the N-type well and one N-type FET formed in the P-type well. In FIG. 4, the CMOS converter includes one N-type well formed of a P-type substrate, one P-type well formed in the one N-type well, one N-type FET formed in the one P-type well and one P-type FET formed in the N-type well.

FIGS. 5 and 6 of Yonemoto illustrate source follower circuits. In FIG. 5, the source follower circuit includes one N-type well formed in a P-type substrate, two P-type wells formed in the N-type well and two N-type FETs formed in the two P-type wells. In FIG. 6, the source follower circuit includes one N-type well formed in a P-type substrate, one P-type well formed in the N-type well and two N-type FETs formed in the P-type well.

FIG. 7 of Yonemoto illustrates an embodiment of a semiconductor device applied to a NAND circuit. FIG. 7 shows one P-type well formed in one N-type well, two N-type FETs formed in the P-type well and two P-type FETs formed in the N-type well. The NAND logic circuit includes two N-type FETs and the two P-type FETs. A ground potential is supplied to the P-type well and a power source potential is supplied to the N-type well.

Yonemoto, however, fails to disclose at least two first well regions of a second conductivity type formed in a semiconductor substrate of a first conductivity type, and at least one second well region of the first conductivity type formed in the at least two first well regions.

In addition, Yonemoto fails to disclose semiconductor elements formed in the at least two first well regions and the at least one second well region, and a memory circuit comprising the semiconductor elements.

Furthermore, Yonemoto fails to disclose at least two first well regions of a second conductivity type formed on the at least two first well regions, respectively, which have different functions.

In the absence of these claimed arrangements, the Yonemoto patent cannot anticipate nor even render obvious the subject matter recited in independent claims 41, 42, 56 and 62. Thus, independent claims 41, 42, 56 and 62 and all claims dependent therefrom are allowable.

CONCLUSION

In view f the foregoing amendments and remarks, Applicant respectfully submits that this application is in condition for allowance and requests early notice to that effect.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at the Washington, D.C. telephone number 202 637-3615 to discuss the steps necessary for placing the application in condition for allowance.

Respectfully submitted,

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